

### **Amendments to the Claims**

This listing of claims will replace all prior versions, and listings of claims in the application:

#### **Listing of Claims:**

Claim 1 (Previously Presented): A semiconductor device comprising:

    a silicon substrate,

    a first conductive type impurity region provided in the silicon substrate, the first conductive type impurity region having an upper surface being exposed at one main surface of the silicon substrate,

    a second conductive type polysilicon plug provided in connection with the upper surface of the first conductive type impurity region to form a PN junction, and

    a wiring connected to a top of the second conductive type polysilicon plug,

    wherein an impurity density of the first conductive type impurity region is a value of  $1.0 \times 10^{15} \text{ cm}^{-2}$  and an impurity density of the second conductive type polysilicon plug is a value within a range of  $5.0 \times 10^{14} \text{ cm}^{-2}$  to  $5.0 \times 10^{15} \text{ cm}^{-2}$ .

Claim 2 (Previously Presented): The semiconductor device according to claim 1, wherein the impurity density of the first conductive type impurity region is equal to the impurity density of the second conductive type polysilicon plug.

Claim 3 (Previously Presented): The semiconductor device according to claim 1, wherein an upper surface of the silicon substrate and the upper surface of the first conductive type impurity region are along a same plane.

Claim 4 (Previously Presented): The semiconductor device according to claim 1, wherein the second conductive type polysilicon plug has a PN junction plug portion forming the PN junction with the first conductive type impurity region, and a wiring connection portion formed continuously and integrally with the PN junction plug portion and connected to the wiring.

Claim 5 (Previously Presented): The semiconductor device according to claim 1, wherein the second conductive type polysilicon plug has a PN junction plug portion forming the PN junction with the first conductive type impurity region and is connected to the wiring.

Claim 6 (Previously Presented): The semiconductor device according to claim 1, wherein each of the upper surface of the first conductive type impurity region and a bottom of the second conductive type polysilicon plug has a same profile.

Claim 7 (Previously Presented): The semiconductor device according to claim 1, wherein the PN junction is formed only along one planar surface.

Claim 8 (Canceled)

Claim 9 (Original): The semiconductor device according to claim 1, wherein the first conductive type is N conductive type and the second conductive type is P conductive type.

Claim 10 (Previously Presented): The semiconductor device according to claim 1, wherein the first conductive type is P conductive type and the second conductive type is N conductive type.

Claim 11 (Currently Amended): A semiconductor device comprising:  
a silicon substrate;  
an impurity region of a first conductive conductivity type formed in the silicon substrate, the impurity region having only an upper surface thereof exposed from the silicon substrate;  
a first insulating film formed on the silicon substrate, the first insulating film including a first opening over the upper surface of the impurity region;  
a polysilicon plug of a second conductivity type formed in the first opening in contact with the impurity region and on an upper surface of the first insulating film;  
a second insulating film formed on the polysilicon plug and on the upper surface of the first insulating film, the second insulating film having a second opening over the

polysilicon plug; and

    a conductive wiring layer formed in the second opening in contact with the polysilicon plug and on an upper surface of the second insulating film.

Claim 12 (Previously Presented): The semiconductor device according to claim 11, wherein the conductive wiring layer is aluminum.

Claim 13 (Previously Presented): The semiconductor device according to claim 11, wherein a surface area of the upper surface of the impurity region is substantially equal to a cross-sectional area of the first opening.

Claim 14 (Previously Presented): The semiconductor device according to claim 11, wherein an impurity concentration of the impurity region is substantially equal to an impurity concentration of the polysilicon plug.

Claim 15 (Previously Presented): The semiconductor device according to claim 11, wherein an impurity concentration of the impurity region is substantially  $1.0 \times 10^{15} \text{ cm}^{-2}$ , and an impurity concentration of the polysilicon plug is within a range of  $5.0 \times 10^{14} \text{ cm}^{-2}$  to  $5.0 \times 10^{15} \text{ cm}^{-2}$ .

Claim 16 (Currently Amended): The semiconductor device according to claim 11, wherein the first conductive conductivity type is n type and the second conductive conductivity type is p type.

Claim 17 (Currently Amended): A semiconductor device comprising:

    a silicon substrate;

    an impurity region of a first conductive conductivity type formed in the silicon substrate, the impurity region having only an upper surface thereof exposed from the silicon substrate;

    a first insulating film formed on the silicon substrate, the first insulating film including a first opening over the upper surface of the impurity region;

    a polysilicon plug of a second conductivity type formed in the first opening in contact with the impurity region;

    a second insulating film formed on an upper surface of the first insulating film, the second insulating film having a second opening over the polysilicon plug; and

    a conductive wiring layer formed in the second opening in contact with the polysilicon plug and on an upper surface of the second insulating film.

Claim 18 (Previously Presented): The semiconductor device according to claim 17, wherein the conductive wiring layer is aluminum.

Claim 19 (Previously Presented): The semiconductor device according to claim 17, wherein a surface area of the upper surface of the impurity region is substantially equal to a cross-sectional area of the first opening and a cross-sectional area of the second opening.

Claim 20 (Previously Presented): The semiconductor device according to claim 17, wherein an impurity concentration of the impurity region is substantially equal to an impurity concentration of the polysilicon plug.

Claim 21 (Previously Presented): The semiconductor device according to claim 17, wherein an impurity concentration of the impurity region is substantially  $1.0 \times 10^{15} \text{ cm}^{-2}$ , and an impurity concentration of the polysilicon plug is within a range of  $5.0 \times 10^{14} \text{ cm}^{-2}$  to  $5.0 \times 10^{15} \text{ cm}^{-2}$ .